3D Integrated eWLB /FO-WLP Technology for PoP & SiP

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Abstract

Embedded Solder On Pad (eSOP) PoP, and Laser [illegible] PoP have proliferated to meet the increasing market demand [4].

3D eWLB-PoP offers significant advantages in thin profile and lower cost compared to current PoP technologies, particularly for mobile or tablet applications. 3D eWLB-PoP [illegible] package e.g. enabling [illegible] stacked PoP e.g. [illegible] after top memory package using body thickness of [illegible]. Table 1 [illegible] the proposition of 3D eWLB-PoP technology [5].

Electrical Performance of 3D eWLB-PoP and fcPoP

The RLC parasitic values for eWLB-PoP and fcPoP were extracted by computer simulation using commercial 3D electromagnetic field solver. The parameters of the package were extracted by using ANSOFT [illegible]. Simulated results are compared in RLC parasitic value and S-parameter. The simulation modeling design was carried out in functional device on the single package to see the performance in real application. In 3D simulation work, a few critical pins were selected and studied, such as clock, DDR data and Data pin.

Table 2. Electrical parasitic values of RL of eWLB-PoP and fcPoP @ 1GHz. :

Net	Inductance, L (nH)			Resistance, R (mΩ)		
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Δ
-72%	1	1.77	[illegible]	[illegible]	[illegible]	[illegible]
-88%	3.08	0.42	-86%	2	2.08	0.24
-62%	3.48	1.12	-68%	3	1.51	0.57
-77%	2.68	0.66	-75%	4	1.08	0.25

For signal integrity study with specific design, the eWLB showed more than [illegible] dB better cross-talk than fcPoP due to thinner Cu RDL and lower, shorter interconnection length shown in Figure 3. Also smooth Cu RDL surface of wafer fab process contributed significantly to the conductance of [illegible]

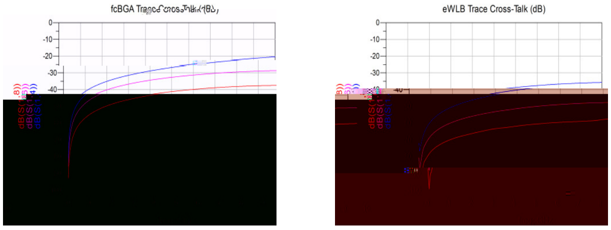

Figure 3. The cross-talk with frequency of signal routing of (a) flipchip and (b) eWLB.

Board Level Reliability of 3D eWLB-PoP/SiP

For board level reliability test, the eWLB PoP [illegible] assembled with top package were pre-assembled with top memory and mounted on the PCB. For PoP assembly, [illegible] body thickness FBGA top package were assembled separately [illegible] and wire bonding process and finally pre-assembled on the eWLB PoP [illegible] top package. [illegible] eWLB PoP assembled package e.g. [illegible] in e.g. after ML on PCB. The test vehicles were tested in JEDEC TCoB and drop reliability test condition.

Table 4 [illegible] 3D eWLB PoP board level reliability of JEDEC TCoB and drop test result of the device and [illegible] and Figure [illegible] The first TCoB failure [illegible] cycle. Drop reliability performance [illegible] and no failure after [illegible] drop. These test results [illegible] excellent board level reliability of 3D eWLB PoP.

Table 3. Board Level Reliability Test Results of 3D eWLB-PoP/SiP

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103	Pass
TCo[illegible]	[illegible]C JESD22-A10[illegible]	[illegible]

2/2um Line Width and Spacing with 3-L RDL [6]

One of the greatest challenges facing wafer level packaging at present is the capability of routing and interconnecting high I/O fine pitch [illegible] RDL redistribution layer to signal and supply I/O's to the reduced footprint [illegible] the eWLB required line width and spacing of [illegible] μm for the eWLB application to support the high pitch of the [illegible] 4[illegible]. Finer line width and spacing are critical for further design flexibility and better electrical performance improvement. For dual-side interconnect of high I/O or multi-die, finer line critical for multi die design and routing flexibility.

Figure 4 shows [illegible] L/L RDL in the eWLB FO WLP. Micrograph shows uniform and well defined micro structure. Cu RDL thickness and CD were also well controlled. Extended design of finer and complex L/L with [illegible] process development, it verified of robust process of fine RDL fabrication using current [illegible] equipment and process flow.

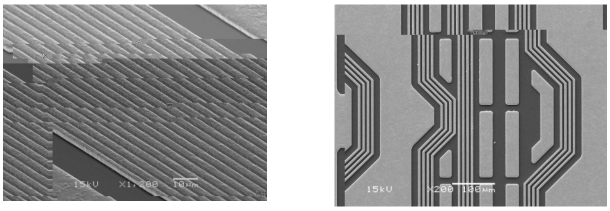

Figure 4. SEM micrographs of 2/2um LW/LS RDL.

3D eWLB SiP / Module

The eWLB FO WLP in 3D configuration has received considerable customer interest for memory and advanced application processor by virtue of the higher routing density and form factor reduction. The requirements for SiP integration is also a growing trend for advanced application processors, MEMS and sensors in IoT. eWLB is also a cost effectively versatile advanced silicon die partitioning for increased performance and integration in a reduced form factor [7].

Figure 5 shows 3D eWLB-PoP modules which have a number of discretes in the top package and are placed on the bottom eWLB-PoP to form a 3D-SiP module. This package profile of [illegible] e.g. [illegible] of [illegible] ^{2} discretes of inductors and capacitors or MLCC were removed from the motherboard and relocated in the top package for reduction in the space required on the motherboard. The embedded discretes are also more power effective when they are close to the device, which significantly improves the power electric performance while providing power saving in package.

Functional samples were prepared with power management integrated circuit (PMIC) as shown in Figure 5. [illegible] ^{2} package size is [illegible] 4.4 [illegible] with die and discretes on top. This 3D eWLB-SiP demonstrated more than [illegible] power efficiency performance compared to other embedded package technology and this is representative of significantly better packaging solution.

Figure 5. Photographs of 3D SiP eWLB-PoP with discretes on interposer or top package of discretes.

MEMS/Sensor eWLB

eWLB FOWLP in a 3D configuration has received consideration due to its lower interest for memory and advanced application processors by virtue of its higher routing density and form factor reduction. The requirements for SiP integration is also a growing trend for advanced application processors, RF modules, MEMS and sensors in IoT. eWLB is also a cost effectively versatile advanced silicon die partitioning for increased performance and integration in a reduced form factor [7].

Figure 6 shows eWLB sensor which was miniaturized from original side by side LGA package. The 3D vertical interconnection and multi-die stacking provide lower footprint reduction and enable thinner [illegible] lower cost MO solution. The thinner body size [illegible] provide or [illegible] are typically good fit for sensor devices such as temperature monitoring and environment sensors. Since sensor devices typically require the same [illegible] composition ASIC and MEMS sensing [illegible] silicon, advanced eWLB FOWLP has shown solution can enhance the [illegible] capacity [illegible] grid array LGA and [illegible] grid array BGA. eWLB PoP footprint [illegible] compatible [illegible] as there is no substrate [illegible]. The package architecture enables routing on both sides of the package by embedding direct [illegible] through the top of the die of the package. The top MEMS device is stacked through [illegible] and the die-free wafer processing, using [illegible] and [illegible] with [illegible] and reflow on the ASIC in the eWLB top package. This eliminates the need for die attach, wire bonding, wire, protecting [illegible] top and also the typical [illegible] cap or molded package [illegible] surface cavity, reducing the typical interposer or die free for routing. Therefore, 3D eWLB-SiP offers smaller footprint, simplified supply chain of lower BOM, reduced [illegible] total cost [illegible] compared with [illegible] the manufacturing process [8].

Figure 6. 3D eWLB for MEMS/Sensor Devices[8].

III. Conclusions

Wafer level technology effectively accommodates fine foundry technology node and provides a strong packaging platform to address performance, form factor, integration and cost requirements. In addition to providing higher I/O density, [illegible] embedded capabilities, and [illegible] improved thermal dissipation in [illegible], 3D eWLB-SiP in packages for advanced wafer level packaging is an alternative for flip chip and embedded package and is becoming choice in the evolving [illegible] use the eWLB FOWLP technology to provide the flexibility of integrating die [illegible] to the co-design process and silicon design optimization, which is significantly critical in [illegible] current market.

Advanced low profile and integrated 3D eWLB-PoP/SiP was developed using eWLB FOWLP technology. 3D eWLB-SiP passed JEDEC standard component level reliability conditions. Board level reliability test of pre-stacked PoP were carried out in JEDEC standard conditions and showed robust reliability in TCoB and drop test. The electrical characterization were also carried out in functional device and signal integrity [illegible] simulation, and showed the enhanced performance of 3D eWLB-PoP compared to conventional fcPoP.

Advanced 3D eWLB technology provides more value for form factor, performance, cost add and improving to enable the next 3D/SiP packaging platform. It can be an attractive application range to support type of emerging mobile, IoT and IoE applications including sensors, MEMS or [illegible] other applications.

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